Linear IC

6-Channel 8-BIT A/D Converter

MB4053

DESCRIPTION

The Fujitsu MB4053 is 6-channel, 8-bit, single-slope A/D converter subsystem designed to be used in a microprocessor based data control system.

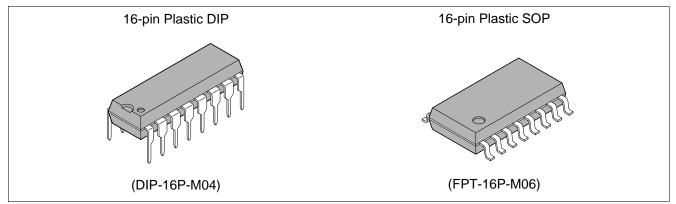
The MB4053 is single monolithic bipolar IC providing a 1 of 8 address decoder, 8-channel analog multiplier, sample and hold, constant current generator, ramp integrator and comparator in a 16-pin package.

This A/D converter subsystems are suitable for a wide range of applications. The resolution required by an application can be obtained by arbitarily selecting a suitable integration time. Also zero offset and full-scale error corrections can be made automatically (auto-zero and auto-calibration) to minimize conversion error.

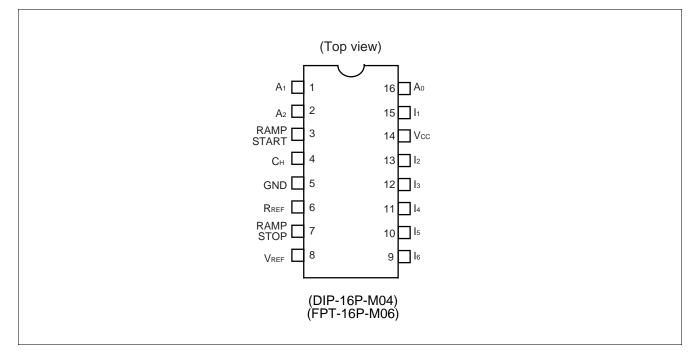
■ FEATURES

- Microprocessor compatible
- Digital input/output: TTL compatible
- · Zero offset and full-scale error correction capability
- · Ratiometric conversion capability
- Available in 16-pin DIP and Flat Package
- Compatible with MC 14443 and μA9708 (DIP package)
- Single power supply: +4.75 V to +15 V
- Excellent linearity: ±0.2% max. error
- Fast conversion time: 300 µs/ch typ.
- Analog input volgage: 0 V to Vcc − 2 V (5.25 V max.)
- Power Dissipation: 25 mW typ. at Vcc = 5 V

PACKAGES



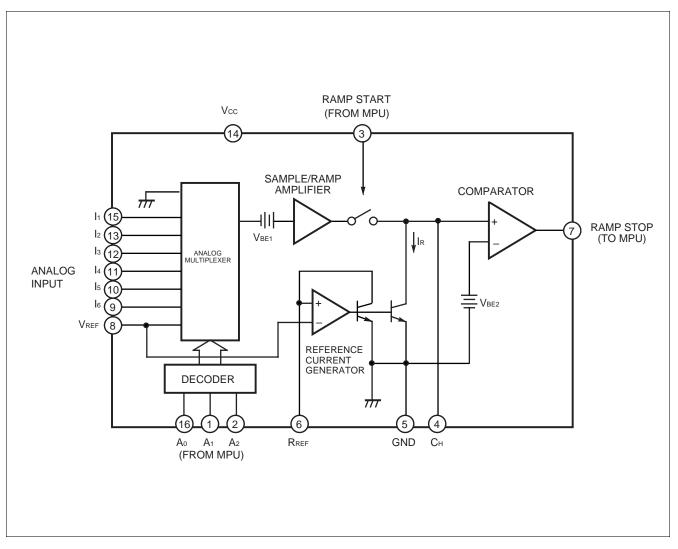
■ PIN ASSIGNMENT



■ PIN DESCRIPTION

Pin no.	Pin name	Symbol	Function
9 to 13 15	Analog input	l₁ thru l₀	Analog inputs for the six channels. One of the 6 is selected by a specific bit pattern on A_0 to A_2 .
16 1 2	Channel selection input	A0 A1 A2	Input for selecting an analog input channel. Either GND, one of channels I ₁ to I ₆ or V _{REF} is selected by a specific bit pattern on the 3 inputs.
3	RAMP START signal input	RAMP START	A/D conversion start signal input. RAMP START $(1 \rightarrow 0)$ Ramp time start signal input. RAMP START $(0 \rightarrow 1)$
7	RAMP STOP signal output	RAMP STOP	Indicates that C _H is charged over comparator reference voltage V _{BE2} . RAMP STOP (0 \rightarrow 1) A/D conversion end signal (C _H discharged to comparator reference voltage). RAMP STOP (0 \rightarrow 1)
4	Ramp capacitor pin	Сн	Pin for externally connecting the ramp capacitor. The value of C _H in conjunction with V _{REF} and R _{REF} establishes the ramp time.
8	Reference voltage supply pin	Vref	Reference voltage supply pin. This is the reference voltage source for determining the discharge current and the analog reference voltage for full-scale factor correction. When the channel selection input is set 111, this pin is selected for channel conversion. The full-scale factor is corrected using the conversion results. The voltage at this pin must be set to (GND + 2 V) to (V _{cc} – 2 V) and 5.25 V or less.
6	Reference	Rref	Pin for external reference resistance for setting the discharge current.
	resistance pin		The external resistance is connected between the power source pin (V _{cc}) and the reference resistance pin (R _{REF}). The discharge current is, then, $I_R = (V_{CC} - V_{REF})/R_{REF}$.
14	Power supply	Vcc	Power supply pin
5	Ground	GND	Ground pin This pin is grounded. When the channel selection input is set to 000, this terminal is selected for channel conversion. The zero offset is corrected using the conversion results.

■ BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rat	Unit		
Falameter	Symbol	Min.	Max.		
Power supply voltage	Vcc	—	18	V	
Digital input voltage	Vind	-0.5	+30	V	
Digital output voltage when off	Vон	-0.5	+18	V	
Analog input voltage	Vina	-0.5	+30	V	
Output current		lo	—	10	mA
Storago tomporaturo	Ceramic	Tstg	-55	+150	°C
Storage temperature	Plastic		-55	+125	°C

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol		Unit		
Farameter	Symbol	Min.	Min. Typ.		Unit
Power supply voltage	Vcc	4.75	5.0	15	V
Reference voltage*	Vref	2.0	—	5.25	V
Ramp capacity	Сн	300	—	—	pF
Reference current	lR	12	—	50	μA
Analog input voltage	VIA	0	—	Vref	V
Output current	lo	—	—	1.6	mA
Operating temperature	Та	-40	—	+85	°C

* : 2 V \leq Vref \leq Vcc - 2 V

WARNING: Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

ELECTRICAL CHARACTERISTIC

(Vcc = 4.75 V to 15 V, Ta = -40°C to +85°C)

Parameter	Symbol	Value			Unit	Remarks	
Faranieter	Symbol	Min.	Тур.	Max.	Unit	Remarks	
Conversion error	EA	_	±0.2	±0.3	%	*1	
Linearity error	Er	_	±0.08	±0.2	%	*2	
Analog input current	Ів	_	-50	-250	nA		
Crosstalk between any two channels	Vcr	60			dB	*3	
Multiplexer input offset voltage	Vosm	—	2.0	4.0	mV		
Conversion time	tc	_	296	350	μs/ch	See "■MEASURMENT CIRCUIT" Analog input: 0 thru V _{REF} C _H = 3300 pF, I _R = 50 μA	
Acquisition time	t∧	_	20	40	μs	See "∎MEASURMENT CIRCUIT" Сн = 1000 pF ^{*4}	
Acquisition current	la	150			μΑ		
Ramp start delay time	to	_	100		ns		
Multiplexer address time	tм	_	1		μs		
Digital high level input voltage	Vін	2.0			V		
Digital low level input voltage	VIL	—	—	0.8	V		
Digital low level input current	lı∟	_	-5	-15	μA	VIL = 0.4 V	
Digital high level input current	Ін	_		1	μA	Vін = 5.5 V	
High level output current	Іон	_	—	10	μA	Vон = 15 V	
Low level output voltage	Vol	—	—	0.4	V	lo∟ = 1.6 mA	
Power supply current	Icc	—	5	10	mA		

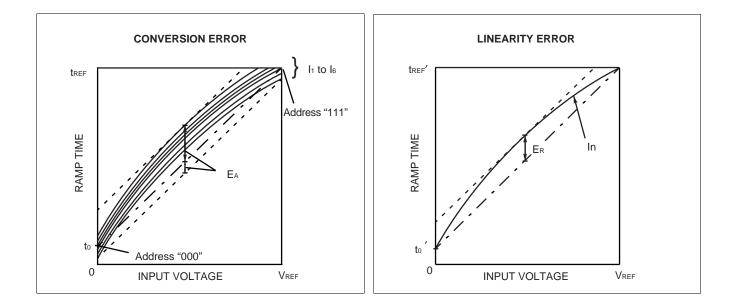
A minus sign (–) prefixing a current value indicates that the current flows from the IC to the external circuit.

*1: Conversion error: For all channels, deviation from a straight line between two points obtained by channel addresses 000 (0 scale) and 111 (full scale).

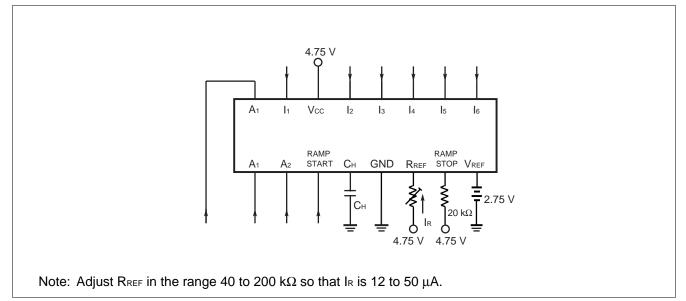
*2: Linearity error; Deviation from a straight line between the 0 and full scale points for each channel.

*3: Crosstalk between channels: Voltage change V_{CH} of C_H terminal occurring when an input voltage of a channel is changed by ΔV_1 while another channel is already charged (RAMP START = 0). This calculated by $20\log \frac{\Delta V_{CH}}{\Delta V_1}$

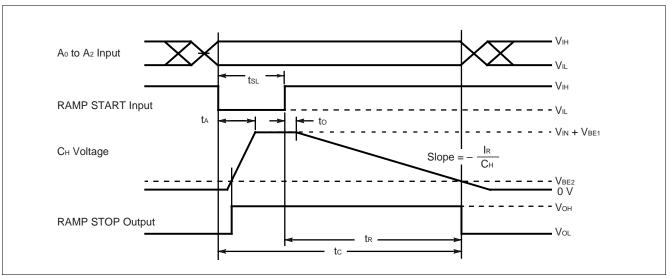
*4: Acquisition time: Sum of multiplexer delay time, RAMP START delay time, and time required to charge the selected input voltage to the ramp capacitor.



■ MEASURMENT CIRCUIT



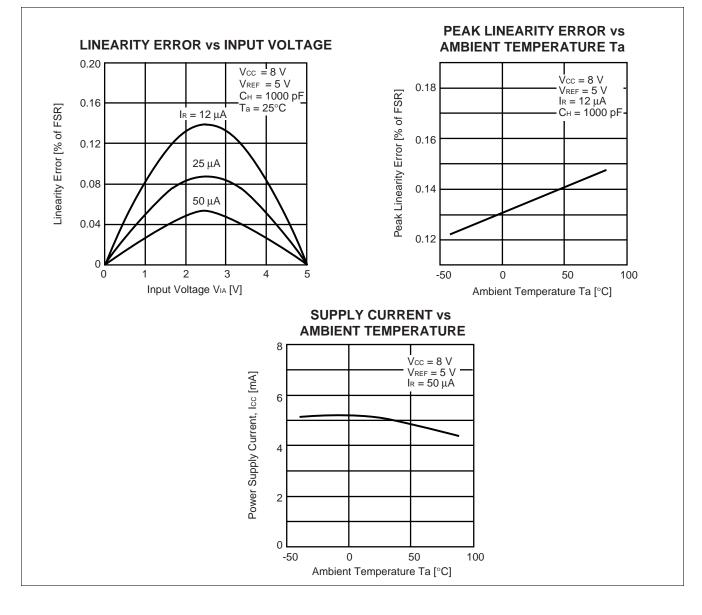
DIAGRAM



■ CHANNEL SELECTION

Inj	put address I	line	Selected analog input	
A 2	A 1	Ao	Selected analog input	
0	0	0	GND	
0	0	1	I 1	
0	1	0	2	
0	1	1	la	
1	0	0	4	
1	0	1	15	
1	1	0	16	
1	1	1	VREF	

■ TYPICAL CHARACTERISTICS



OPERATION DESCRIPTION

Refer to BLOCK DIAGRAM, and DIAGRAM. Address inputs A_0 to A_2 are used to select the analog input to be converted, (one of the six analog inputs I_1 to I_6). The RAMP START input is switched from a logic 1 to a logic zero. This causes the external ramp capacitor C_H to charge at a fixed rate. (Note 1) until it reaches the sum of the selected analog input voltage and a constant offset voltage V_{BE1} . The RAMP STOP output (open-collector switches from a logic 0 to logic 1 when the voltage on C_H reaches the comparator reference voltage V_{BE2} . The RAMP START input is switched back to a logic 1 after C_H is completely charged. This disconnects the analog input from C_H and allows it to be gin discharging at a fixed rate (Note 2). When the voltage on C_H reaches the comparator reference voltage V_{BE2} the RAMP STOP output switches back to a logic 0. This completes a conversion cycle for 1 channel.

The time between the RAMP START input switching $(0\rightarrow 1)$ and RAMP STOP output switching $(1\rightarrow 0)$ is the RAMP TIME tr. This would be directly proportional to the analog input voltage for the ideal situation where there was no comparator switching level error, leakage, switching delay times or effect of the impedance of the internal reference current source. tr can be calculated for the ideal case as follows:

$$t_{R} = V_{IN} \times \frac{C_{H}}{I_{R}}$$

Where: VIN = Analog input voltage to be measured

$$C_{H} = \text{External ramp capacitor}$$
$$I_{R} = \frac{V_{CC} - V_{REF}}{R_{REF}}$$

This ramp time is converted to a digital representation by counting tR with the microprocessor. If a small error can be tolerated, the A/D conversion software can be reduced and the conversion time minimized by omitting corrections.

Notes:

*1 Charge slope =
$$\frac{I_A - I_R}{C_H} \ge \frac{150 \ \mu A - I_R}{C_H}$$

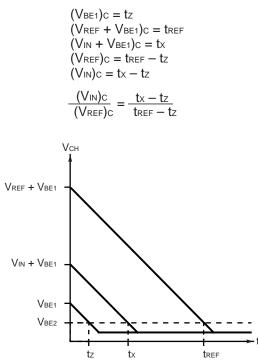
Where: IA is the acquisition current whose value is determined from the circuit constant in the IC.

*2 Discharge slope =
$$-\frac{I_R}{C_H}$$

ZERO OFFSET AND FULL-SCALE FACTOR CORRECTIONS

High precision conversions can be achieved by correcting for zero offset and full scale factor as follows:

The channel select address (A_0 to A_2) is set to 000. Ground (GND) is selected (internally) as the analog input and converted. This results in ramp time t_R. Next the address is set to 111. V_{REF} is selected (internally) and converted. This results in ramp time, t_{REF}. Finally the desired analog input (one of I₁ to I₆) is selected and converted. This results in ramp time t_x. This conversion sequence is arbitrary and the GND and V_{REF} conversions are not needed each time a channel is converted but only as required for calibration. The relationships between the inputs and ramp times are shown below.



The conversion error can then be minimized by using the above results in the expression below to calculate the corrected analog input voltage.

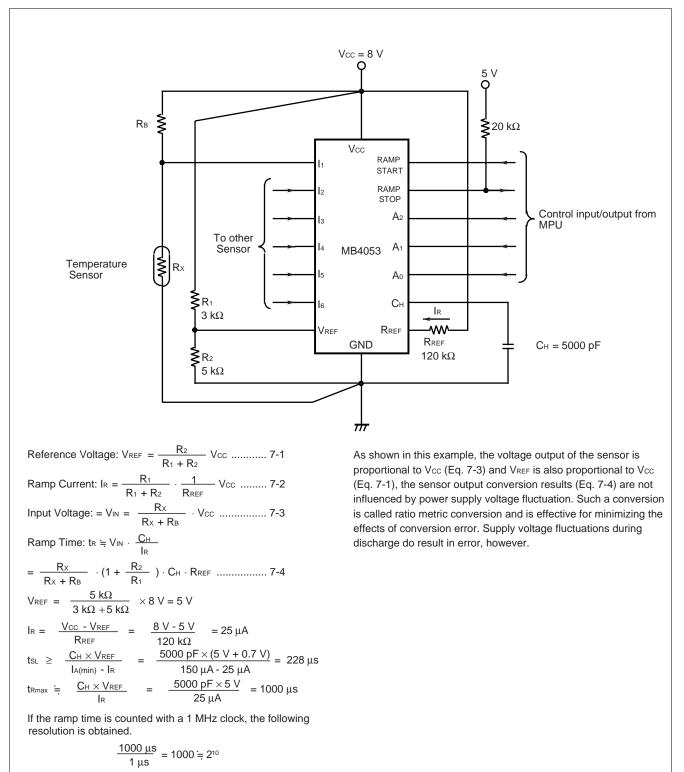
$$(V_{IN})_{C} = (V_{REF})_{C} \times \frac{t_{x} - t_{z}}{t_{REF} - t_{z}}$$

Where: V_{IN} = Analog input voltage to be measured V_{REF} = Reference voltage V_{BE1} = Shift voltage in sample/ramp amplifer V_{BE2} = Threshold voltage of comparator V_{CH} = C_H voltage

The GND and VREF conversion sequence is arbitary, the GND and VREF conversions not being needed each time a channel (I1 to I6) is converted.

APPLICATION EXAMPLES

Examples of analog voltage (0 to 5 V) A/D conversion with 10-bit resolution are shown in "PEAK LINEARITY ERROR vs AMBIENT TEMPERATURE Ta" and "SUPPLY CURRENT vs AMBIENT TEMPERATURE".



USAGE PRECAUTIONS

- 1. Shince the impedance of the ramp capacitor pin is approximately 30 M Ω (high), a resistance must not be connected in paralleled with this input. A ramp capacitor with no leakage must be used.
- 2. At $V_{IN} = 0$ V, t_R has a finite value.
- 3. Since RAMP STOP is an open collector output, an external pull-up resistor is required. (For example, when a 20 k Ω external pull-up resistor is used.)
- 4. All digital inputs/output are TTL compatible.
- 5. The time from RAMP START input switching $(0 \rightarrow 1)$ to RAMP STOP output switching $(1 \rightarrow 0)$ is ramp time tR.

6.
$$t_{SL} \ge t_A (max) = \frac{C_H}{150 \ \mu A - 1_R} \times (V_{REF} + 0.7 \ V)$$

7.
$$t_{R} \doteq \frac{C_{H}}{I_{R}} \times V_{IN}, t_{R} (max) \doteq \frac{C_{H}}{1_{R}} \times V_{REF}$$

8. Ir =
$$\frac{V_{CC} - V_{REF}}{R_{REF}}$$

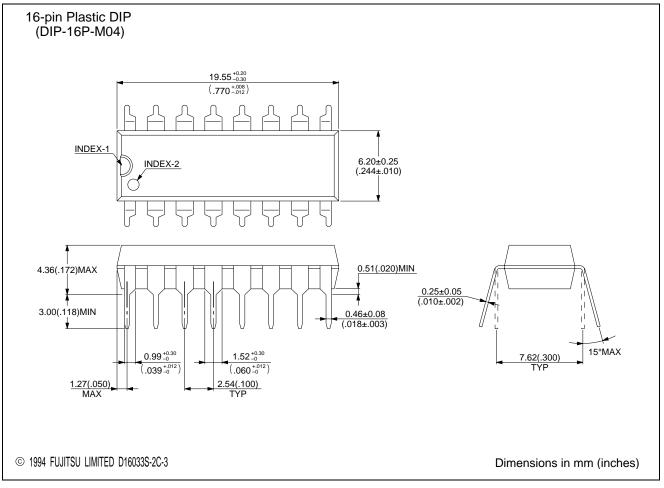
- 9. $2 \text{ V} \leq \text{V}_{\text{REF}} \leq (\text{V}_{\text{CC}} 2 \text{ V}) \text{ and } \text{V}_{\text{REF}} \leq 5.25 \text{ V}$
- 10. While and analog input voltage is being sampled, channel selection signals A₀, A₁, and A₂ must not be changed for (ts_L).
- 11. When IR is little, Linearity Error extends. However, Linearity Error is ±0.2 [% of FSR] or less in IR (min) = 12 µA.

■ ORDERING INFORMATION

Part number	Package	Remarks
MB4053M	16-pin Plastic DIP (DIP-16P-M04)	
MB4053PF	16-pin Plastic SOP (FPT-16P-M06)	

MB4053

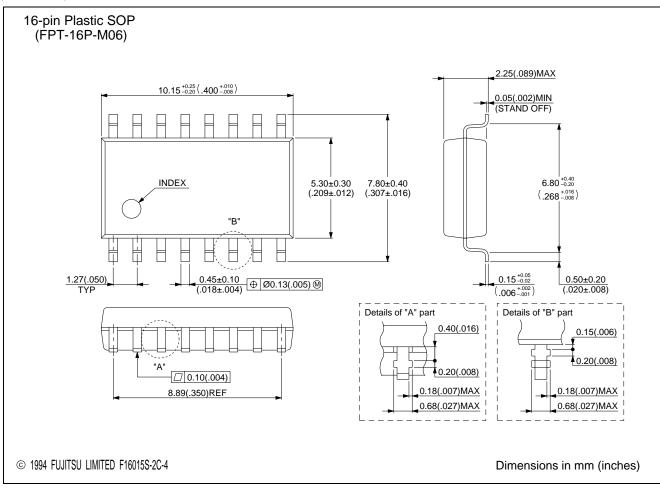
■ PACKAGE DIMENSIONS



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MB4053

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